SPECIFICATION

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[Add-on Card For Wireless Communication With Power-Managing Circuit]

Background of Invention

[0001] 1.Field of the Invention

[0002] The present invention relates to an add-on card for wireless communication with a personal digital assistant (PDA), and more particularly, to an add-on card for wireless communication with a power-managing circuit for managing the power supplied.

[0003] 2.Description of the Prior Art

[0004] Modern electrical technological advancements have vastly decreased the size of a personal computer. Some portable computers are light enough and small enough to be put in a pocket. They are called pocket or palm-sized computers, such as the personal digital assistant (PDA).

[0005] The expansion, or add-on card, is a card which contains electronic devices and is inserted in a socket formed in such a portable personal computer in order to improve its performance or functionality. Recently, the relative socket and the expansion cards have been widely standardized.The socket of the PDA has to provide the current needed by the circuitry of the add-on card for the card to work properly.

[0006] With the increasing popularity of PDAs, there has been a similar increase into researching various functioned add-on cards to improve the PDAs performance. If every add-on card is suitable for the standard socket, the PDA can be relatively low cost and convenient to expand functionality. However, because the power supplied

from the standard socket of the CF card is limited, it limits the add-on cards functionality. The highest current supplied from the standard socket of the PDA is about 550 milliampere (1 milliampere = 1/1000 ampere). If the add-on card needs more current to operate normally than the specification of the standard socket of the PDA provides, the PDA cannot utilize this add-on card to improve its functionality. For example, a desired transient current of an RF circuit for transmitting or receiving the RF signal operating in wireless communication is about 2000 milliampere. Therefore, the RF circuit cannot be located in the add-on card due to the insufficient current of the socket, and the PDA cannot be improved in the field of the wireless communication by using the standard socket of the CF card.

Summary of Invention

[0007] It is therefore a primary objective of the claimed invention to provide an add-on card for wireless communication with a power-managing circuit, which improves a PDAs functionality in wireless communication by storing current supplied from thesocket of the add-on card and then discharging the stored power timely to supply a larger desired transient current for the add-on card, thus circumventing the insufficient current supplied from the socket.

[0008] According to the claimed invention, the add-on card for wireless communication comprises a rectangular housing having an opening formed on an upper side of the rectangular housing, an interface connector located in the opening of the rectangular housing for connecting to a PDA, a power-managing circuit electrically connected to the interface connector for storing power of a first direct current (DC) supplied from the interface connector, and a radio-frequency (RF) circuit enclosed in the rectangular housing and electrically connected to the interface connector for transmitting a RF signal corresponding to an electrical signal from the interface connector or transmitting an electrical signal to the PDA via the interface connector according to a received RF signal. The power-managing circuit is electrically connected to the RF circuit, and when the RF circuit transmits the RF signal, the power-managing circuit provides a second DC to the RF circuit.

[0009] The add-on card in the claimed invention includes the power-managing circuit to adjust the desired power of the RF circuit, so the power can be stored in the power-

storage unit when the RF circuit operates in the low power consumption mode and can be discharged to support the higher desired current when the RF circuit operates in the high power consumption mode.

[0010] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0011] Fig.1 isa schematic diagram of an add-on card for wireless communicationfor use in a PDA according to the present invention.

[0012] Fig.2 is a function block diagram of the add-on card shown in Fig.1.

[0013] Fig.3 is a schematic diagram illustrating current flow magnitude variations of the add-on card shown in Fig.1.

[0014] Fig.4A to Fig.4C are function block diagrams of the add-on card shown in Fig.1 when the add-on card operates in various modes.

Detailed Description

[0015] Please refer to Fig.1. Fig.1 isa schematic diagram of an add-on card for wireless communication 20 for use in a PDA 10 according to the present invention. The PDA 10 includes a touch screen 12A for displaying pictures and accepting input by touch, and a plurality of buttons 12B formed on the PDA 10. The users can touch the touch screen 12A and the buttons 12B to operate the PDA 10. In order to match the add-on card 20, the PDA 10 further includes an opening 14B comprising an expansion socket 18B located in the insert opening 14B. The add-on card 20 in the present invention, is covered with a rectangular housing 21 having an opening 14A formed on an upper side of the rectangular housing 21, and an interface connector 18A corresponding to the expansion socket 18B located in the opening 14A. When the add-on card 20 is inserted into the opening 14B of the PDA 10, the interface connector 18A will be connected to the expansion socket 18B.

[0016]

Please refer to Fig.2. Fig.2 is a function block diagramof the add-on 20 connected

to the PDA 10. A processing circuit 32 is located in the PDA 10 for controlling the PDA 10, such as storing information, executing programs and processing data, etc. The touch screen 12A for displaying pictures and the buttons 12B are electrically connected to the processing circuit 32, and the users can touch the touch screen 12A and the buttons 12B to operate the processing circuit 32 of the PDA 10. In addition, the PDA 10 has a battery 30 for supplying desired power for operating the PDA 10. In order to connect to the add-on card, a data terminal 26B for transmitting an electrical signal, a power terminal 34B, and a ground terminal 36B for transmitting a direct current (DC) power are located in the expansion socket 18B of the PDA 10.

[0017] The add-on card 20, having a radio-frequency (RF) circuit 24 enclosed in the rectangular housing 21 for transmitting and receiving a RF signal, is used to increase the functionality of the PDA 10 in the present invention. The interface connector 18A of the add-on card 20 has a data terminal 26A, a DC power terminal 34A and a ground terminal 36A corresponding to the data terminal 26B, the power terminal 34B, and the ground terminal 36A of the expansion socket 18B, respectively. When the expansion socket 18B is connected to the interface connector 18A, the data terminal 26A and the data terminal 26B, the power terminal 34B and the DC power terminal 34A, and the ground terminal 36A and the ground terminal 36B are electrically connected with each other, respectively. Therefore, the processing circuit 32 can exchange the electrical signal with the RF circuit 24 via the data terminals 26A and 26B, the power supplied from the battery 30 can be transmitted to the add-on card 20 via the DC power terminals 34A and 34B, and the ground terminals 36Aand36B.

[0018] The operating method of the add-on card 20 is described below. When the users utilize wireless communication using the PDA 10, the processing circuit 32 transmits an electrical signal 28A to the RF circuit 24 of the add-on card 20 via the data terminals 26A and 26B. The RF circuit 24 transmits a RF signal 28B corresponding to the electrical signal 28A in a wireless manner. On the other hand, when the add-on card 20 receives a RF signal 28B, the RF circuit 24 generates the electrical signal 28A, according to the received RF signal 28B, to the processing circuit 32 via the data terminals 26A and 26B. The RF circuit 24 of the add-on card 20 transmits, receives, and processes the RF signal so as to expand the wireless communicationfunctionality of the PDA 10.

[0019] Please refer to Fig.3. Fig.3 is a schematic diagram illustrating desired current flow magnitude variations of the RF circuit 24 while it operates in various modes. The transverse axis in Fig.3 is time and the vertical axis is a current flow magnitude. The RF circuit 24 is the principal operating circuit when the add-on card 20 is used for wireless communication. In order to operate the RF circuit 24 normally, the desired power of the RF circuit 24 must be supplied. Because a larger transmission power is needed when the RF circuit 24 transmits the RF signal, the desired current magnitude (power) of the RF circuit 24 is increased. The time periods T1, T3, and T5 shown in Fig.3 are durations when the RF circuit 24 transmits the RF signal, and the desired current flow magnitude I_a shown in Fig.3 of the RF circuit 24 is larger in these conditions. On the other hand, when the RF circuit 24 does not transmit the RF signal but receives the RF signal or is in a down time, a lower current flow magnitude I_b shown in Fig.3 is desired.Time periods T2, T4, and T6 are durations when the RF circuit 24 receives the RF signal or is in a down time. However, the expansion socket 18B of a normal CF card is unable to supply asufficient current flow magnitude to the RF circuit 24 while the RF circuit 24 transmits the RF signal. The current flow magnitude I_c shown in Fig.3 is the current flow magnitude that the expansion socket 18B supplies to the RF circuit 24 via the power terminals 34B and 34A. As shown in Fig.3, although the current flow magnitude I_c supplied from the expansion socket 18B can supply the desired current flow magnitude I_b (time periods T2, T4 and T6) to the RF circuit 24 when the RF circuit 24 receives the RF signal or is in a down time, it is unable to supply the desired current flow magnitude I_a (time periods T1, T3 and T5) when the RF circuit 24 transmits the RF signal. In order to solvethis problem, the add-on card 20 further includes a power-managing circuit 22 in the present invention.

[0020] Please refer to Fig.2; the power-managing circuit 22 includes a resistor R electrically connected between a node N1 and a node N3, a power-storage unit 38 and a bypass circuit 40. The power-storage unit 38 is a capacitor C with a large capacitance with the two ends of the capacitor C connected to node N3 and node N6, respectively. The bypass circuit 40 comprises a P-type metal-oxide semiconductor (MOS) transistor M. The source of the transistor M is electrically connected to node N4, forming an input terminal of the bypass circuit 40. The drain of the transistor M is

electrically connected to node N5, forming an output terminal of the bypass circuit 40. The gate of the transistor M is electrically connected to node N7. In the power-managing circuit 22, the node N1 is connected to the DC power terminal 34A, the node N2 is connected to the RF circuit 24, the ground terminals 36Aand 36B, and the nodes N6 andN7 are electrically connected to the ground terminals of the power-managing circuit 22 and the RF circuit 24.

[0021]

Please refer to Fig.4A to Fig.4C. Fig.4A to Fig.4C are function block diagrams of the power-managing circuit 22 of the present invention operating in various modes. As shown in Fig.4A, before the add-on card 20 operates, the power stored in the power-storage unit 38 is probably low, and the voltage of the node N3 is also low. When the add-on card 20 starts to operate, the higher voltage supplied from the DC power terminal 34A charges thelower voltagednode N3. At this time, the PDA 10 provides a first DC I1, as an arrow shown in Fig.4, flowing through the power terminals 34B and 34A into the add-on card 20. The first DC I1 flows into the two currents $I1_a$ and $I1_c$ at node N1 and node N2, respectively, charging the capacitor C of the power-storage unit 38, and a current $I1_d$ bypassing node N2 flows into the RF circuit 24. The current $I1_a$ flowing from node N1 to node N3 through the resistor R charges the capacitor C of the power-storage unit 38. The resistor R limits the current flow magnitude of the current $I1_a$ to prevent the voltage of node N3, at the beginning of charging, from increasing suddenly to the voltage of node N1,destroying the capacitor C. On the other hand, the voltage difference between node N4 (source) and node N7 (gate) of the transistor M is not large enough to open the transistor M.However, an equivalent diode D formed due to the reserved bias between node N5 and node N4 of the transistor M (between the drain and the source of the transistor M) will be opened because the voltage of node N5 is larger than the voltage of node N3 allowing the current $I1_c$ toflow through the drain and the source of the transistor M into node N3. The current $I1_c$ (together with the current $I1_a$) charges the power-storage unit 38. As the power stored in the power-storage unit 38 increases, the voltage of the node N3 increases gradually, and the magnitude of the currents $I1_a$ and $I1_c$ decrease. When the power-storage unit 38 is saturated, the voltage of the node N3 and the voltage of the node N2 are substantially equivalent, and the current flow magnitudes of the currents $I1_a$ and $I1_c$ decrease substantially to zero. The

equivalent diode D will be closed because the voltages of node N5 and node N2 are equivalentsimultaneously. However, the voltage difference between the source (node N4) and the gate (node N7, ground terminal) of the transistor M is larger than the threshold voltage of the transistor M and the transistor is opened in a low current mode. During the above-mentioned charging period, the current $I1_d$ bypassed from the current I1 supplies continuously the desired power of the RF circuit 24. Whenfirst beginning to operate the add-on card 20, an elementary procedure with low power consumption is necessary, such as receiving relative RF signals. At this moment, the desired current of the RF circuit 24 is low enough that the first DC I1 not only satisfies the desired current of the RF circuit 24 by using the current $I1_d$, but also charges the power-storage unit 38 by using the currents $I1_a$ and $I1_c$. When the add-on card 20 finishes the elementary procedure in the wireless communication, the power of the power-storage unit 38 is charged enough.

[0022] Please refer to Fig.4B. Fig.4B is a function block diagram of the power-managing circuit 22 of the present invention operating in a high power consumption mode. When the RF circuit 24 operates in the high power consumption mode and starts to transmit the RF signal, the first DC I1 supplied from the DC power terminal 34A is insufficient to supply the desired power of the RF circuit 24, so that the capacitor C of the power-storage unit 38 discharges to provide external current and power to the RF circuit 24. When the RF circuit 24 starts to transmit the RF signal and the desired current is increased suddenly, the voltage of the node N2 decreases slightly because the current flow magnitude of the DC power terminal 34A is insufficient. The voltage of the node N2 (together with the node N1 short-circuited with the node N2) is lower than the voltage of the node N3 after the power-storage unit 38 is charged enough, and the capacitor C of the power-storage unit 38 starts to discharge, generating a second DC I2 (shown in Fig.4B). The second DC I2 splits into two currents $I2_a$ and $I2_b$ at node N3. The current $I2_a$ flows from node N3 to node N1, and the current $I2_b$ flows from node N3, through node N4 and node N5, into the first DC I1 supplied from the DC power terminal 34A. The transistor M is opened in a high current mode between node N4 (source) and node N5 (gate), and then an equivalent resistance is formed between node N4 and node N5 after the transistor M is opened.The resistance value of the equivalent resistance is lower than that of the resistor R so that the

current flow magnitude of the current $I2_a$ is larger than that of the current $I2_b$. Briefly, the current flow magnitude of the total current I3 provided at the node N2 to the RF circuit 24 is a sum of the first DC I1, the current $I2_a$, and the current $I2_b$; namely the sum of the current flow magnitudes of the first DC I1 and the second DC I2. In the present invention, the capacitance C of the power-storage unit 38 is a capacitor with a large capacitance. The charge quantity stored in the capacitor C is a multiplication of its capacitance and voltage. If the voltage of node N3 decreases slightly, appropriate charges will be discharged from the capacitor C to form the sufficient second DC I2. The current I3 provided from the first DC I1 and the second DC I2 are sufficiently suitable for the desired current when the RF circuit 24 transmits the RF signal.

[0023]

Please refer to Fig.4C. Fig.4C is a function block diagram of the power-managing circuit 22 operating in a low power consumption mode. When the RF circuit 24 receives the RF signal or is in a down time , the necessary current for the RF circuit 24 is decreased. As shown in Fig.3, when the RF circuit 24 receives the RF signal or is in a down time, the desired current is lower than the first DC I1 supplied from the DC power terminal 34A. During this time, the first DC I1 not only satisfies the desired power of the RF circuit 24, but also chargesor recharges the power-storage unit 38. Therefore, when the RF circuit 24 switches from high to the low consumption modes, the voltage of the DC power terminal 34A is normally higher than the voltage of the node N3, and the first DC I1 charges the capacitor C and provides the current I4 to the RF circuit 24 keeping the desired current. When the RF circuit 24 operates in the high consumption mode, the voltage of the power-storage unit 38 decreases slightly due to discharge. When the RF circuit 24 switches to the low consumption mode, the first DC I1 provides a current $I4_a$ at the node N4 to recharge the power-storage unit 38. At this moment, the reversed bias equivalent diode D between the source and the drain of the transistor will not open because the voltage difference between node N4 and node N5 is not sufficient, so that the power-storage unit 38 will not receive current via the bypass circuit 40 at node N2. It only will be charged by the current $I4_a$ bypassed from node N4 to prevent the power-storage unit 38 from charging too much from the first DC I1 to affect the normal current supplied from the first DC I1 to the RF circuit 24 in the low consumption mode. As the current $I4_a$ charges

continuously, the power of the power-storage unit 38 will be re-supplied so that the voltage of the node N3 increases. When the voltage of the node N3 increases to the voltage of the DC power terminal 34A, the current flow magnitude of the current $I4_a$ decreases to zero. The power of the voltage of node N3 is now saturated. When the RF circuit 24 switches from the low power consumption mode to the high power consumption mode, the power-storage unit 38 provides the second DC to supply the power again, as shown in Fig.4B.

[0024]

In summary, when the RF circuit 24 needs more power to transmit the RF signal, the power-managing circuit 22 discharges the power stored in the powerstorage unit 38,compensating for the insufficient power supplied from the DC power terminal 34A, so that the RF circuit 24 can operate normally in the high power consumption mode. On the other hand, when the RF circuit 24 operates in the low power consumption, the excess power supplied from the DC power terminal 34A can be stored in the power-storage unit 38 of the power-managing circuit 22 for supplementing the insufficient current of the DC power terminal 34A when the RF circuit 24 operates in the high power consumption mode. For example, when the RF circuit 24 transmits the RF signal and needs more current, about 2 amperes, the RF circuit 24 operates in the high power consumption mode about 0.001 second (i.e. each time period T1, T2 and T3 shown in Fig.3 is about 0.001 seconds). However, the greatest current flow magnitude of the PDA 10 via the DC power terminal 34A is about 0.5 ampere. In the present invention, the capacitor C of the power-storage unit 38 has a large capacitance, such as 2 faradays. If the voltage of node N3 decreases 0.00075 volts lower than the voltage of node N1, about 1.5 amperes can be provided during the needed 0.001 seconds (i.e. the second DC I2 shown in Fig.4B). In the present invention, the resistance value of the resistor R is about 0.2 ohm, and a resistance value of the equivalent resistance formed between node N4 and node N5 of the transistor M is about 0.002 ohm, so that a great part of the second DC bypasses to the current $I1_a$ flowing through node N2 to the RF circuit 24. On the other hand, when the RF circuit 24 operates in the low power consumption (i.e. the time periods T2, T4 and T6 shown in Fig.3),the time period, about 0.01 seconds, is longer.The first DC I1 supplied from the DC power terminal 34A can provide the power to charge the power-storage unit 38 of the power-managing circuit 22 during this time, as shown

in Fig.4. The power-storage unit 38 can also utilize the battery capable of charging to achieve the improvement of the present invention.

[0025] In prior art technology, the current supplied from the standard expansion socket of the PDA is insufficient to support the desired current of the RF circuit when the RF circuit operates in the high power consumption mode, so that users can not utilize the simple and low cost add-on card to improve the functionality of the PDA. In contrast to the prior art, the add-on card in the present invention includes a power-managing circuit to adjust the desired power of the RF circuit so the power can be stored when the RF circuit operates in the low power consumption mode and discharged to support the higher desired current of the RF circuit when the RF circuit operates in the high power consumption mode. Therefore, the PDA can utilize the add-on card to expand its functionality in the field of wireless communication. The advantages of the present invention are described as follows. First, the present invention continues using the conventional expansion socket of the CF card. Although the current supplied from the expansion socket is insufficient to support the high power consumption mode of the add-on card, the add-on card in the present invention utilizes the power-managing circuit to adjust the desired power to avoid the problem. This allows users to improve the functionality of the PDA by using this expansion socket without the need for designing new PDAs. In addition, the power-managing circuit re-supplies the power automatically when the RF circuit operates in the low power consumption, and the user does not have to charge the add-on card or change a battery, which is convenient and efficient. The power-managing circuit is not only utilized in the present invention, but also in the add-on card for other functionality.

[0026] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.